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Effect of geometry and film thickness on self-cooling of SIN junctions intended for particle detector applications

O.B. Drury[1,2], J.P. Castle[1,2], S.R. Golwala[2], J. Jochum[2], B. Neuhauser[1,2],
C.A. Mears[3], W.C. Fellers[1,2], F.P. Lipschultz[1,2], and B. Sadoulet[2]
[1] *Thin Film Laboratory, San Francisco State University, Dept. of Physics and Astronomy*
[2] *NSF Center for Particle Astrophysics, University of California at Berkeley*
[3] *Physics and Space Technology Directorate, Lawrence Livermore National Laboratory*

Abstract

An SINIS structure should self-cool significantly if it is biased properly because the tunneling current removes the more energetic electrons from the normal electrode. However, the junction may be reheated if these hot quasiparticles do not escape the junction region before they either backtunnel or emit recombination phonons which may be absorbed in the normal electrode. We are studying this effect by using our full-wafer $Al/Al_2O_3/Cu$ photolithographic process to produce SINIS structures with geometries which eliminate quasiparticle bottlenecks. Fabrication quality is monitored by analyzing IV data at low bias voltage. Self-heating is evaluated by exposing the devices to 6 keV X-rays and using a SQUID array to measure the variation of current pulse height with bias voltage. For devices having the same junction area, narrow junctions on thick superconducting base layers self-heat less than square junctions on thin base layers. For devices having the same shape, junctions with smaller dimensions self-heat less.

1 Introduction

San Francisco State University (SFSU), the NSF Center for Particle Astrophysics (CfPA) at the University of California at Berkeley, and the Physics and Space Technology Directorate at Lawrence Livermore National Laboratory (LLNL) are developing practical thin film fabrication techniques and auxiliary structures for the purpose of building advanced detectors based upon superconductor-insulator-normal (SIN) tunnel junction technology. We are exploring ways of coupling a variety of energy absorbers to SIN junctions, which are ultrasensitive thermometers for the electrons in the normal metal. We want to exploit the fact that a carefully designed SIN device will self cool significantly if it is biased properly because the tunneling process removes the more energetic electrons from the normal electrode. This unique capability may allow SIN-based detectors to achieve the high sensitivity associated with operation at ultralow temperature while using a simpler and cheaper refrigerator having a relatively high base temperature.

2 Tunneling Processes

Tunneling from the normal electrode to the superconductor transfers both charge and energy across the junction as shown in Figure 1. If the bias voltage V is in the range $0<V<\Delta/e$, the gap in the superconductor density of states blocks most of the final states for hole tunneling from the normal film but only some of the final states for electron tunneling, so net charge transport is possible. Electrons

which tunnel from the normal electrode into the superconducting electrode have energy $E - E_f > \Delta - eV$. Replacement electrons supplied by the bias network are introduced at the Fermi level. Thus the tunneling process actually decreases the average energy of the normal electron system and causes it to cool [1].

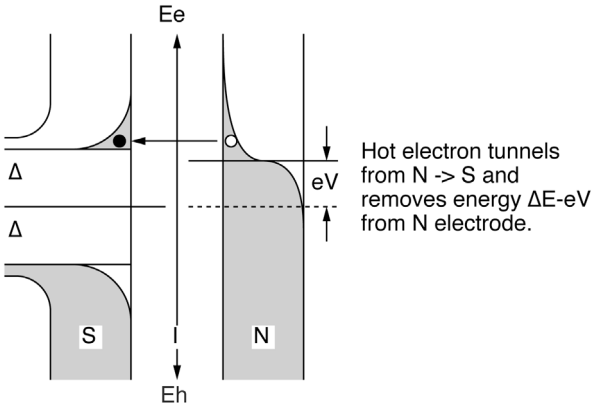

Figure 1: Density of states diagram for N to S tunneling in an SIN junction.

Tunneling from the superconductor to the normal metal transfers no net charge, but it does transport energy as shown in Figure 2. The symmetric populations of thermally generated quasielectrons and quasiholes are equally likely to tunnel in the same direction due to the fact that the normal metal density of states does not have a gap which would block either tunneling process. Consequently there is no net electrical current. However, quasielectrons and quasiholes which tunnel from the superconductor into the normal metal together transfer energy $(\Delta - eV) + (\Delta + eV) = 2\Delta$ into the normal electrode [2].

Electrons which have tunneled from the normal metal into the superconductor are in general called quasiparticles. If these hot quasiparticles do not escape from the tunneling region quickly, they may reheat the normal electrode by backtunneling or by recombining and emitting a 2Δ phonon which may be absorbed in the normal electrode. Energy balance in the normal electrode of an SIN junction has been modeled extensively by J. Jochum, who has also considered exchange of energy between electrons and phonons at a rate proportional to $(T_e^5 - T_{ph}^5)$ where T_e is the electron temperature and T_{ph} is the phonon temperature [3].

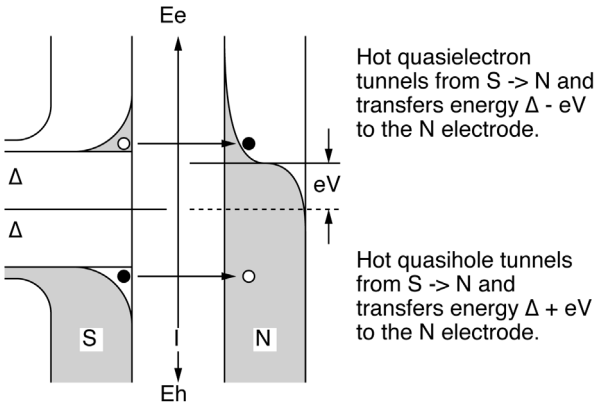

Figure 2: Density of states diagram for S to N tunneling in an SIN junction.

3 Self-Cooling SINIS Devices

In order to exploit the self-cooling potential of an SIN device a method must be found for removing hot quasiparticles from the junction region. One promising approach can be inferred from the structure of an SINIS device with submicron junctions in which the normal electrode cooled to 100 mK while the bath temperature remained at 300 mK [4]. The impressive cooling capability of this symmetric design was attributed in large part to the absence of a metallic SN biasing contact to the normal electrode. However, we have found that SINIS devices having 100 μm x 100 μm junctions self-heat rather than self-cool because of a quasiparticle bottleneck in the junction region beneath the normal electrode [5]. We surmise that a critical requirement for effective self-cooling is that the tunneling regions must be small relative to the quasiparticle mean free path so that hot quasiparticles entering the superconducting electrode quickly diffuse away from the junction region before recombining or backtunneling.

Difficult direct-write electron beam exposure and lift-off patterning techniques were used to make the submicron junctions that demonstrated the principle of SIN microrefrigeration. It is challenging to apply that technology to create SIN-based detectors having auxiliary structures such as thick energy absorbing films, quasiparticle traps, and charge collection electrodes on nonstandard substrates. We are adapting our full-wafer fabrication process to create SIN devices which are large enough (2-5 μm) to be produced by standard optical lithographic techniques but which nevertheless self-cool because they have built-in escape routes for hot quasiparticles and recombination phonons. We have started with the simplest possible structure by using narrow normal electrodes over thick, large-area superconducting base layers which act as quasiparticle diffusers as depicted in Figure 3. For clarity the base layer thickness is shown to be greater than the junction width, but such a favorable aspect ratio is not likely to be achieved in practice.

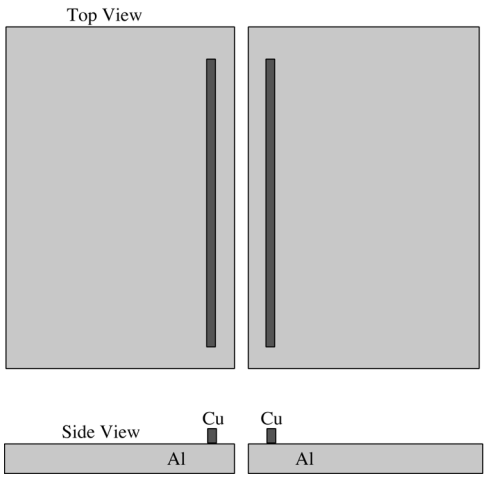

Figure 3: Narrow junctions on thick base layers for optimal junction cooling (wiring layer not shown).

4 Device Fabrication

Our devices are fabricated in the Thin Film Laboratory at San Francisco State University. We have developed a full-wafer process for making $Al/Al_2O_3/Cu$ SIN tunnel junctions [6]. This process allows us to produce robust, high-quality SIN devices having predictable tunneling properties and very few defects because the junction is formed without exposing the tunneling barrier to the atmosphere at any time. Figure 4 summarizes the steps required to make a series pair of SIN junctions; this structure significantly simplifies fabrication because both electrical leads are extensions of the superconducting base layer.

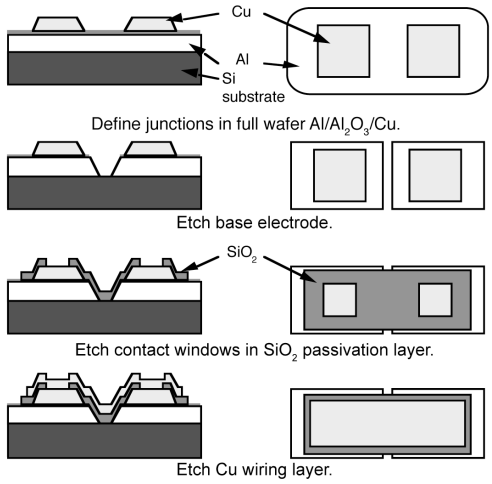

Figure 4: Full wafer process for making $Al/Al_2O_3/Cu$ SIN series pair.

For an ideal junction pair with no shunt conductance $I = (V/2R_n)\,(2\pi\Delta / k_BT)^{1/2} \exp(-\Delta / k_BT)$ if $eV \ll k_BT \ll \Delta$. Thus a plot of log I *vs* 1/T measured with low excitation voltage would be approximately linear as indicated by the dotted line on Figure 5. Actual data is shown for two pairs of $(100\ \mu m)^2$ junctions separated by about six millimeters on the same chip. The fact that the data is nearly the same for the two devices suggests that the junctions have identical tunnel barriers and dimensions and that the excess current at low temperature is due to trapped flux rather than to process-induced defects which shunt the tunnel barrier. Repeated thermal cycling causes leakage current to increase in some junctions.

In order to test our hypothesis that dispersal of hot quasiparticles and recombination phonons can be controlled by junction geometry and base layer film thickness, we prepared chips with sets of SINIS devices having junctions with equal areas but different shapes progressing from squares to very long, narrow rectangles. The tunnel barriers on a given chip are identical because they were created simultaneously as part of the full-wafer SIN structure. Therefore the normal state resistance, Rn, varies inversely with junction area. Junctions on separate chips having SINIS pairs with different base layer thicknesses were oxidized under identical conditions so that they also should have closely matched barriers. These chips allow us to compare performance of devices having the same tunneling properties but different areas, shapes, or base layer thicknesses.

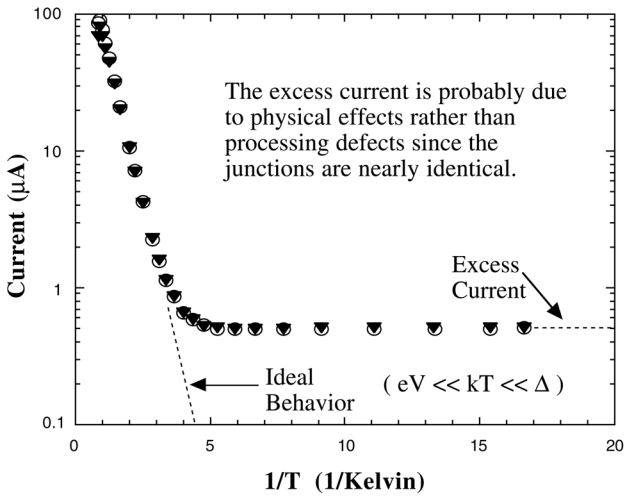

Figure 5: Log I vs 1/T for two junctions on the same chip. Bias voltage is 10 μV.

The chips described in this paper have either a 2000 Å or a 3000 Å aluminum base layer. The tunnel barriers in all of the devices have a specific resistance of approximately $0.9\ k\Omega \times \mu m^2$ (i.e. R_n= 0.09 ohm for a 100 μm x 100 μm junction). The copper counterelectrodes are 1000 Å thick and the copper wiring layers are either 4000 Å or 4500 Å thick. Junction dimensions for particular devices are given at appropriate points in the next section.

5 Results

The most straightforward method of determining whether the normal electrode of an SINIS device is cooling would be to measure the temperature directly with an auxiliary SIN junction. However, incorporation of that structure significantly complicates the fabrication process. For that reason we used an alternative method to analyze our junctions. We cooled the devices to nominal temperatures below 125 mK in an adiabatic demagnetization cryostat at U.C. Berkeley and irradiated them with 6 keV X-rays from an ^{55}Fe source. We voltage-biased each junction pair and measured current pulses with 200-SQUID series arrays manufactured by HYPRES, Inc., operated in an open loop mode [7]. Ideally, if the normal electrons absorb energy ΔE, the tunneling current would increase by $\Delta I = \left(\Delta E / \gamma W T\right)\left(\partial I / \partial T\right)_v$ where W is the volume of the normal electrode, γ is the Sommerfeld constant, and the derivative $\left(\partial I / \partial T\right)_v$ is the responsivity of an SIN junction. At a fixed temperature the maximum current pulse amplitude is obtained when the device is biased on the peak of the responsivity curve. As the normal electrode is cooled, the optimum bias point approaches the gap voltage (2Δ/e for a series SIN pair) and the pulse height increases as shown in Figure 6. Ideally, then, the relative temperatures of the

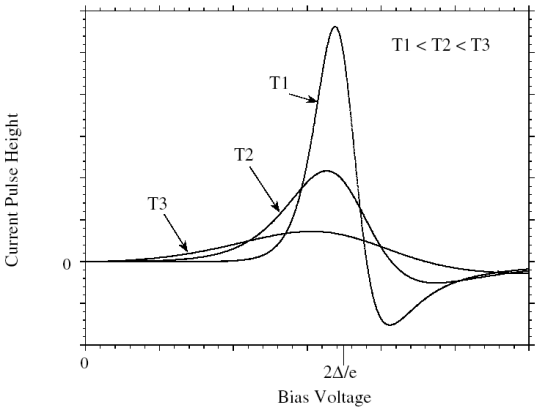

Figure 6: Ideal current pulse height for a SIN device at various temperatures.

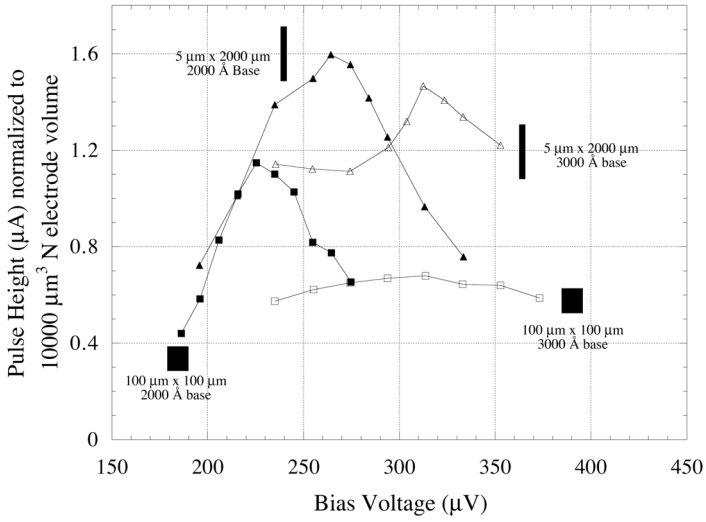

Figure 7: Variation of pulse height with bias voltage for devices having different junction shapes and base-layer thickness.

normal metal electrons in different junctions can be estimated by comparing optimum bias voltages and pulse heights.

Figure 7 is a graph of normalized pulse height as a function of bias voltage for the 100 μm x 100 μm junctions and the 5 μm x 2000 μm junctions on each of two chips with base layer thicknesses of 2000 Å and 3000 Å, respectively. The indicated bias voltages have not been corrected for loading of the bias network by the junction, but the effects are small and the ordering of points is correct. For a particular base layer thickness the long, narrow junction has a higher optimum bias voltage and larger pulses than the square junction. For a particular shape the junction on the thicker base layer has a higher optimum bias voltage. All of these effects are consistent with the conjecture that the use of narrow junctions on thick base layers reduces the quasiparticle bottleneck beneath the junction. The puzzling feature is that the pulses in the junctions on the 3000 Å base layer chip are smaller than the pulses in the corresponding junctions on the 2000 Å base layer chip. Some of the discrepancy is due to the fact that the devices with smaller pulses had larger leakage conductance which shunts the SQUID input coil and therefore reduces sensitivity. There also may be as yet unidentified errors in corrections for differences in the normal electrode and wiring layer volume of each device.

Figure 8 is a graph of normalized pulse height as a function of bias voltage for the 100 μm x 100 μm junction and the 50 μm x 50 μm junction on a chip with a 2000 Å base layer. The smaller junction has a higher optimum bias voltage which, we believe, is a reliable indicator that the smaller junction is colder. Once again, however, there is a pulse height deficit that we are still investigating.

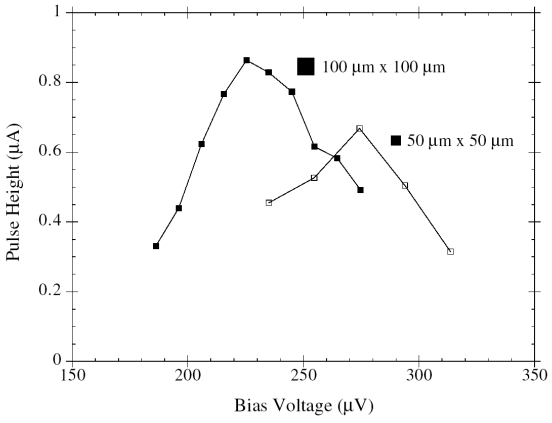

Figure 8: Variation of pulse height with bias voltage for devices with different junction areas.

Our next goal is to produce 3 μm wide junctions on 1 μm thick base layers. We are developing self-aligned junction passivation structures in order to minimize junction widths. We also are perfecting bilayer wet etching and directional dry etching processes which allow us to control sidewall slopes so that step coverage will not be a limiting factor when we build SIN devices with thin (i.e. low heat capacity) normal metal wiring layers.

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