Preparation and characterization of $Al/Al_2O_3/Cu$ SIN tunnel junctions microfabricated with a full wafer process

J. P. Castle[a,b], M. F. Cunningham[a,b], B. Neuhauser[a,b], S. Golwala[b], F. P. Lipschultz[a,b,d], A. Barootkoob[a,b], O.B. Drury[a,b], M. Frank[c], J. Jochum[b], S.E. Labov[c], C.A. Mears[c], B. Sadoulet[b], A. Slepoy[a,b], and D. A. Yale[a,b]

[a] Thin Film Laboratory, San Francisco State Univ., Dept. of Physics and Astronomy

[b] NSF Center for Particle Astrophysics, University of California at Berkeley

[c] Laboratory for Experimental Astrophysics, Lawrence Livermore National Laboratory

[d] Dept. of Physics, University of Connecticut at Storrs

We have developed a "full wafer" process for producing $Al/Al_2O_3/Cu$ superconductor-insulator-normal (SIN) tunnel junctions for use as X-ray and phonon sensors. We describe microfabrication details and present I-V data.

1. INTRODUCTION

Superconductor-insulator-normal (SIN) tunnel junctions, which are ultrasensitive thermometers for the normal metal electrons, can be used as X-ray or phonon detectors if the junctions are coupled to appropriate absorbers [1]. We are developing photolithographic techniques for fabricating SIN junctions and related structures because these methods offer superior dimensional control, alignment accuracy, and topological flexibility compared to shadow masking techniques.

Initially we built $Al/Al_2O_3/Cu$ edge-masked devices in which the tunneling regions were defined by openings in an insulating layer separating the base electrode from the upper electrode [2]. These SIN devices were robust and stable, and junctions produced on the same wafer had very similar tunneling characteristics. However, it was difficult to control the junction formation process because the tough native oxide on the aluminum layer had to be removed by ion bombardment before the desired barrier oxide was grown and the copper layer was deposited.

A potentially more reliable method of fabricating SIN junctions with specified tunneling properties is to adapt the "full wafer" process developed for $Nb/Al_2O_3/Nb$ superconductor-insulator-superconductor (SIS) devices [3]. These are made by coating the entire substrate with an SIS structure without breaking vacuum. Barrier formation is very well controlled and virtually immune to contamination. The key requirements for implementing a full wafer process are (1) selective etching of the upper electrode with respect to the base electrode and (2) passivation of the edges of the tunneling region.

2. OUR FULL WAFER SIN PROCESS

We fabricate our devices in the San Francisco State University (SFSU) Thin Film Laboratory. Our principal deposition system is a load-locked UHV sputtering system.

We are developing our $Al/Al_2O_3/Cu$ full wafer process using series pairs of SIN junctions because both leads can be made from extensions of the superconducting base electrodes. Figure 1 is a schematic of the fabrication steps. First we clean the silicon substrates for five minutes in 4:1 H_2SO_4:H_2O_2 at 90 C, rinse them in deionized (DI) water, dip them in room temperature 50:1 DI:HF to strip the oxidized surface layer, rinse them again in DI, clean them for five minutes in 1:1:5 HCl:H_2O_2:DI at 70 C, and rinse them a final

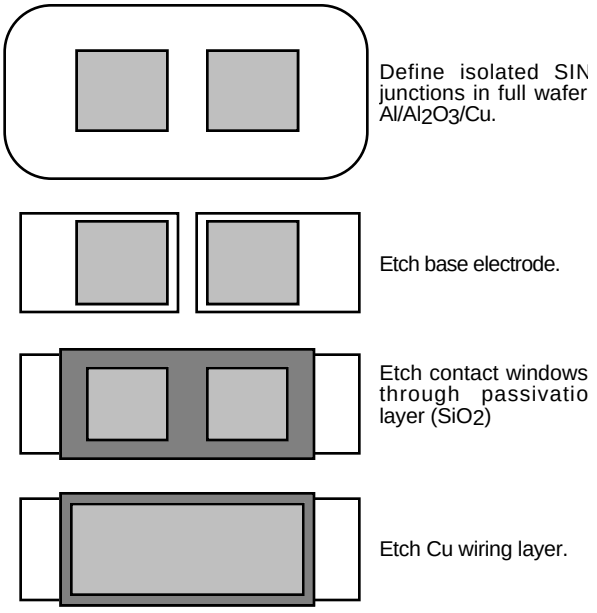

Figure 1: Etching steps for series pairs

time in DI. We DC sputter a 1200 Å aluminum base layer, oxidize the film in the load lock for fifteen minutes at oxygen pressures ranging from 100 milliTorr to 100 Torr, and then DC sputter a 1000 Å copper electrode. We create isolated $(90\mu m)^2$ SIN structures by wet-etching the copper electrode in a room temperature bath of 1 liter:23 ml 10%-HOAc:H_2O_2. This etchant does not attack the aluminum base layer if the H_2O_2 is fresh. We wet-etch the aluminum base electrode and then RF

sputter a 1500 Å SiO_2 passivation layer. We use a CHF_3/O_2 plasma to etch contact windows through the SiO_2 down to the copper electrodes of the junctions. Finally we deposit and pattern a 2000 Å copper wiring layer to make the series connection. An experienced person can complete this procedure in less than twelve hours.

3. DC CHARACTERISTICS

Preliminary low temperature DC data for our first generation of junctions made with the full wafer process was acquired at SFSU in a ^{3}He cryostat. Measurements were extended to sub-100 mK temperatures in adiabatic demagnetization refrigerators at U.C. Berkeley and at Lawrence Livermore National Laboratory (LLNL).

Figure 2 is an IV curve for a typical device at 260 mK. For $eV<<kT<<\Delta$ the current in an SIN series pair is given by the expression

$$I = (V/2R_n)\sqrt{2\pi\Delta/kT}\ \exp(-\Delta/kT)$$

where R_n is the normal resistance of a single junction and Δ is the gap parameter for the superconducting electrode. Thus a plot of log I *vs*. 1/T measured at a

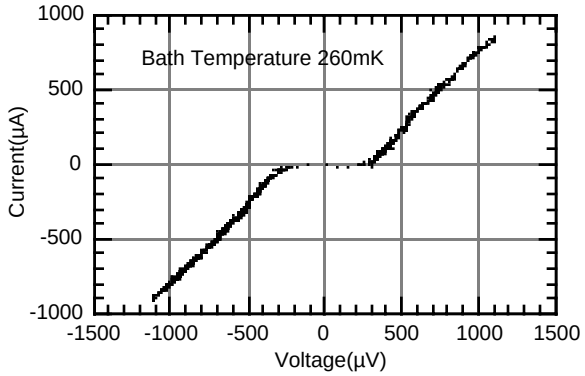

Figure 2: Typical SIN I-V Characteristic

constant small voltage should be nearly linear. In Figure 3 we show this relationship for two typical junction pairs with different normal resistances. Both pairs deviate from ideal behavior at sufficiently low temperature (high 1/T). However, the deviation occurs at lower temperature for the junction with higher R_n. We are not yet certain whether that effect occurs because low resistance junctions self heat more or because their thinner barriers are more vulnerable to defects. Figure 4 is a log-log plot of normal resistance as a function of oxidation pressure with oxidation time held constant at fifteen minutes. This preliminary data fits a power law $R_n \propto P^{0.50}$.

Pulse data from full-wafer SIN series pairs exposed to 6 keV X-rays is presented elsewhere in these proceedings [4].

Pulse data from full-wafer SIN series pairs exposed to 6 keV X-rays is presented elsewhere in these proceedings [4].

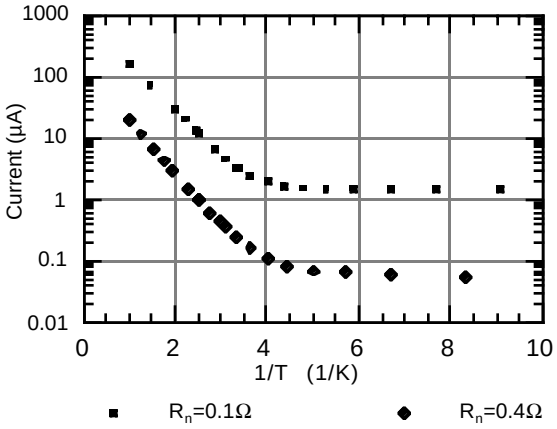

Figure 3: Current @30μV for SIN Junction Pairs

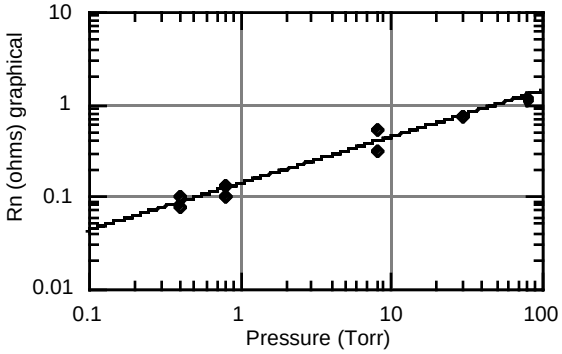

Figure 4: Rn vs. Oxidation Pressure

4. ACKNOWLEDGMENTS

Research at SFSU was funded by NSF grants PHY 90-58517, PHY 94-07930, and PHY 94-14675; and by the NSF Center for Particle Astrophysics subcontract AST-912005. Research at LLNL was performed under the auspices of the U.S. Dept. of Energy contract No. W-7405-ENG-48.

REFERENCES

[1] M. Nahum *et al*, J. Low Temp. Phys. 93 (1993) 733.
[2] D. Chow *et al*, Nucl. Instr. & Meth. A 370 (1996) 57.
[3] M. Gurvitch *et al*, Appl. Phys.Lett. 42 (1983) 472.
[4] M. Cunningham *et al*, these proceedings.